

FIG. 1 (PRIOR ART)

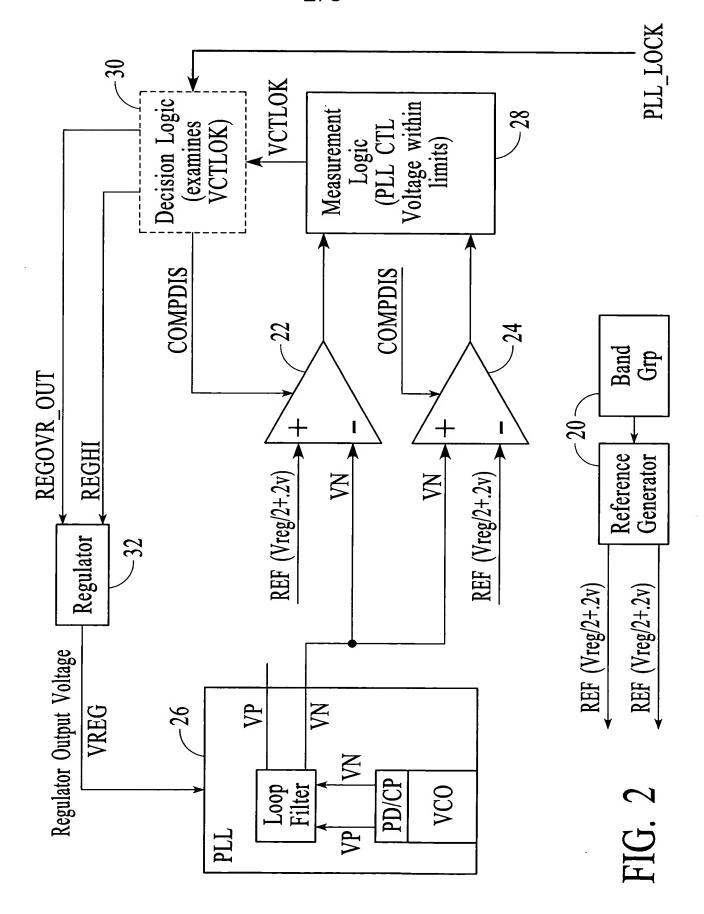


Table 1: REGVHI and REGOVR_OUT Mapping

REGVHI	REGOVR_OUT	Regulator Voltage
0	0	1.1V
0	1	1.2V
1	0	not allowed
1	1	1.3V

If at any time REGOVER IN = '1' then

REGVHI = '0', REGOVR_OUT = '1', COMPDIS = '1', and BLOCK PLLLOCK = '0'.

Else

After reset or power up:

REGVHI = '1', REGOVR_OUT = '1', COMPDIS = '0', and BLOCK_PLLLOCK = '1'.

Wait 150 us.

Sample (VCTLOK ended with internal PLL_LOCK indicator).

If VCTLOK_SAMPLE = '1' then

REGVHI = '1', REGOVR_OUT = '1', COMPDIS = '0', and BLOCK_PLLLOCK = '0'. Stop. Keep outputs the same until next reset.

Else

REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '0', and BLOCK_PLLLOCK = '1'.

Wait 150 us.

Sample (VCTLOK ended with internal PLL_LOCK indicator).

If VCTLOK_SAMPLE = '1' then

REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '1', and BLOCK_PLLLOCK = '0'. Stop. Keep outputs the same until next reset.

Else

REGVHI = '0', REGOVR_OUT = '0', COMPDIS = '1', and BLOCK_PLLLOCK = '1'.

Stop. Keep outputs the same until next reset.

End if

FIG. 3